

# Claims

[c1] What is claimed is:

1.A multi-clock domain logic system comprising:  
a plurality of clock domains corresponding respectively  
to a plurality of clock signals and comprising at least one  
flip-flop group per each clock domain;  
wherein during a scanning test, a scanning test clock  
signal is asynchronously input into the clock domains in  
a predetermined sequence.

[c2] 2.The system of claim 1, wherein the clock domains  
comprises a first clock domain coupled with a first clock  
signal, the first clock domain comprising:  
a first flip-flop group that receives the first clock signal;  
a second flip-flop group; and  
a first logic gate group coupled with the first clock signal  
for generating a first logic signal,  
wherein during the logic operation, the first flip-flop  
group receives the first clock signal as its clock signal,  
the second flip-flop group receives the second clock sig-  
nal as its clock signal, and during the scanning test, the  
scanning test clock signal is asynchronously input into  
the first flip-flop group and the second flip-flop group

in sequence to be their clock signal.

- [c3] 3.The system of claim 2, wherein the first clock domain further comprises:
  - a first delay device coupled with the scanning test clock signal for delaying the scanning test clock signal; and
  - a first multiplexer coupled with the first logic gate group, the first delay device, and the second flip-flop group, for selectively outputting the first logic signal or the delayed scanning test clock signal to the second flip-flop group.
- [c4] 4.The system of claim 2, wherein the first clock domain further comprises:
  - a first delay device coupled with the scanning test clock signal for delaying the scanning test clock signal; and
  - a first multiplexer coupled with the first delay device and the first flip-flop group, for selectively outputting the first clock signal or the delayed scanning test clock signal to the first flip-flop group.
- [c5] 5.The system of claim 2, wherein the first flip-flop group and the second flip-flop group are serially connected in a scan chain.
- [c6] 6.The multi-clock logic system of claim 1, further comprising:

a first clock domain coupled with a first clock signal comprising at least one first flip-flop group; and  
a second clock domain coupled with a second clock signal comprising at least one second flip-flop group,  
wherein during the scanning test, the scanning test clock signal is asynchronously input into the first flip-flop group and the second flip-flop group in sequence to be their clock signal.

- [c7] 7.The system of claim 6, wherein the first clock domain further comprises:  
a first delay device coupled with the scanning test clock signal for delaying the scanning test clock signal; and  
a first multiplexer coupled with the first delay device and the second flip-flop group, for selectively outputting the second clock signal or the delayed scanning test clock signal to the second flip-flop group.
- [c8] 8.The system of claim 1, wherein each flip flop group comprises at least one first unit for selectively outputting a function input signal or a scan input signal.
- [c9] 9.The system of claim 8, wherein the first unit is a scan flip-flop.
- [c10] 10.The system of claim 8, wherein the first unit further comprises:

a first multiplexer for selectively outputting the function input signal or the scan input signal; and  
a first flip-flop for receiving the function input signal or the scan input signal and outputting the function input signal or the scan input signal according to the corresponding clock signal.

[c11] 11. The system of claim 1, wherein the scanning test clock signal is one of the clock signals.

[c12] 12. A multi-clock domain logic system comprising:  
a first clock domain that receives a first clock signal comprising:  
a first flip-flop group that receives the first clock signal;  
a second flip-flop group; and  
a first delay device for outputting a first delayed scanning test clock signal; and  
a second clock domain that receives a second clock signal comprising:  
a third flip-flop group that receives the second clock signal; and  
a second delay device for outputting a second delayed scanning test clock signal,  
wherein during a scanning test, through the first delay device and the second delay device, a scanning test clock signal is asynchronously input into the first flip-flop group, the second flip-flop group and the third flip-flop

group in a predetermined sequence.

- [c13] 13.The system of claim 12, wherein the first delayed scanning test clock signal is prior to or following the second delayed scanning test clock signal.
- [c14] 14.The system of claim 12, wherein the first clock domain further comprises a first logic gate group coupled with the second flip-flop group, for outputting a first logic signal according to the first clock signal; and the second flip-flop group operates according to the first logic signal when logic operation is executed.
- [c15] 15.The system of claim 12, wherein the scanning test clock signal is the first clock signal or the second clock signal.
- [c16] 16.A method of scanning test of a multi-clock domain logic system comprising:  
during a logic operation, operating a first flip-flop group and a second flip-flop group according to a first clock signal or a second clock signal; and  
during a scanning test, operating the first flip-flop group according to a first scanning test clock signal, and operating the second flip-flop group according to a delayed first scanning test clock signal.
- [c17] 17.A method of claim 16, further comprising:

delaying the first scanning test clock signal and outputting the delayed first scanning test clock signal to the second flip-flop group.